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A Reduced Switching Two-Vector MMPC Scheme for MMCs in Medium Voltage Applications

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***Abstract*—A two-vector Modulated Model Predictive Control (MMPC) scheme is proposed in this paper that achieves reduced switching in the output pole voltage of a Modular Multilevel Converter (MMC). This switching state change reduction is significant when compared to the conventional three-vector pulse width modulation (PWM) scheme. The proposed two-vector scheme is generalized for any n-level pole voltage operation and is suitable for digital implementation. The three main control parameters in MMC i.e. output current, inner circulating current and submodule capacitor voltages are satisfactorily controlled while a reduced switching two-vector scheme is applied. The simulation results considering 10 submodules in each arm of 3-ϕ MMC are showcased while feeding power to the medium voltage grid at unity power factor. Hardware results along with transient performance are also incorporated.**

***Index Terms*—Medium voltage MMC, Reduced switching, Two-vector 2N+1 modulation.**

I. Introduction

The distinctive advantages of modularity, ease of scalability, quality output where bulky transformers and filter inductors may be avoided [1], and no need for isolated DC sources have made Modular Multilevel Converter (MMC) a popular choice. MMC has proved its efficacy in high-voltage applications and is making its way into medium-voltage applications [2]–[4]. For proper operation of MMC, the output current, the inner circulating current and the submodule capacitor voltages need to be controlled. A feedback linearization current control strategy is proposed in [5], but linear controllers suffer from a narrow operating stable range and slow transient response. Modulated Model Predictive Control (MMPC) provides faster dynamic response and simpler controller design [6].

The low frequency modulation methods like Nearest Level Modulation (NLM) and Selective Harmonic Elimination (SHE) are popular choice for high voltage applications of MMC. For medium voltage applications, high frequency carrier based comparison pulse width modulation (PWM) methods like phase-shift PWM (PS-PWM) [7], phase-disposition PWM (PD-PWM) [8] and space vector modulation [9] are more effective in providing quality output. The modulation method of MMC can be double reference arm based [10], [11] or single reference direct phase leg based [12] producing 2N+1 pole voltage levels at the output of MMC, where 'N' is the number of submodules in each arm of MMC. The single reference direct phase leg modulation in [12] provides better harmonic performance as it puts the dominant harmonic energies in the odd carrier sideband groups of the pole voltage which eventually gets cancelled in line to line voltage. The complexity of the state machine decoder in [12] is avoided in [13] in generating 2N+1 pole voltage levels at the output. The non-optimal switchings associated with PS-PWM, PD-PWM or space vector modulation based MMC operation increases the switching losses of MMC and may hinder its progress in medium voltage applications.

Some of the notable works which are aimed to reduce the switching losses in MMC are reported in [14]–[17]. In [14], a discontinuous clamping modulation is proposed that may degrade the harmonic performance. A combination of NLM and PS-PWM was proposed in [15] typically suited for high voltage applications. The double reference arm based modulating signals were used in [16] where the signals were clamped for certain intervals. In [17], an active power filter increasing the component count was incorporated to reduce the power loss. The reduced switching frequency sorting algorithm was proposed in [18], [19]. The switching status of the submodule switches has to be known before sorting. These are not generalized and with an increase in the number of submodules there is an increase in the computational complexity. A two-vector model predictive control scheme for a hybrid multilevel converter is proposed in [20] where the switching reduction technique is not investigated.

The two-vector term used in this work is solely used for the application of two vectors per carrier period in the modulation stage. The conventional space vector modulation and 2N+1 PD-PWM implemented as simple carrier based comparison method can be termed as a three-vector scheme. The three vector represents the vertices of a triangle per sector of a regular hexagon two level space vector structure. The main contributions of the paper can be highlighted as

1. A two-vector reduced switching MMPC scheme is proposed that achieves satisfactory control of the parameters for proper operation of MMC.

2. The reduction in switching state change per fundamental period is significant for two-vector scheme when compared to three-vector scheme.

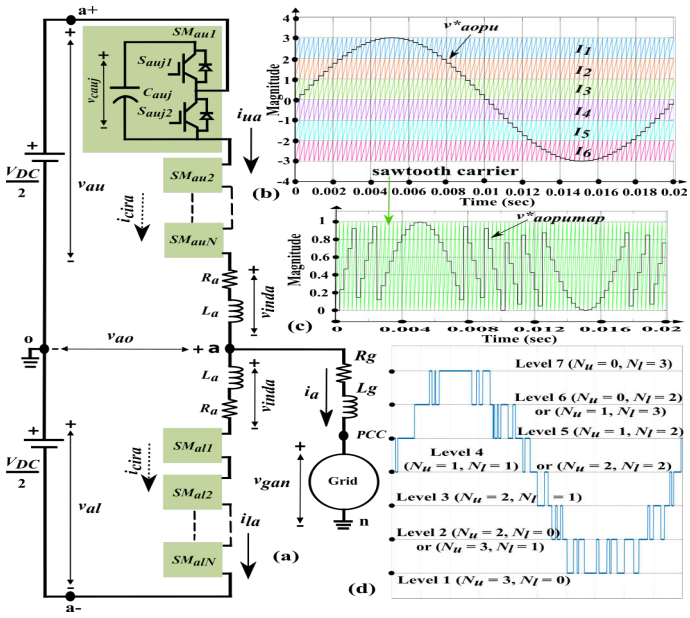

Fig. 1. (a) MMC single phase power circuit schematic with grid interface. (b) Sampled reference pole voltage in per unit along with level shifted sawtooth carrier for N = 3. (c) Pole voltage adjusted for single carrier level digital implementation. (d) Two-vector based simulated pole voltage output levels with arm insertion indices for N = 3.

3. The proposed two-vector scheme is generalized for any n-level pole voltage operation of MMC and is digitally implementable.

II. Control Strategy

A. Modulated Model Predictive Output Current Control

The model predictive control approach in [21] has been extended in this work for grid interface. The single reference pole voltage v_{ao} for 'a' phase is calculated per carrier period to control the output current in that particular phase. Similar analysis holds good for other two phases also. The output pole voltage is the combination of the upper and lower arm half bridge submodule (S_{auj1}, S_{auj2} is the top and bottom switch of the submodule respectively) capacitors inserted in the phase leg of MMC as shown in Fig. 1(a). The high signal to S_{auj1} inserts the capacitor and high signal to S_{auj2} bypasses the capacitor in the arm circuit. The upper and lower arm dynamics of MMC can be written from Fig. 1(a) as

$$-\frac{V_{DC}}{2} + v_{au} + R_a i_{ua} + L_a \frac{di_{ua}}{dt} + v_{ao} = 0 \tag{1}$$

$$\frac{V_{DC}}{2} - v_{al} - R_a i_{la} - L_a \frac{di_{la}}{dt} + v_{ao} = 0 \tag{2}$$

$$i_{ua} = i_a + i_{la} \tag{3}$$

where, v_{au}, v_{al} is the upper and lower arm 'a' phase voltage, i_{ua} and i_{la} is the upper and lower arm current respectively and i_a is the output phase current in Fig. 1(a). Adding (1) and (2), and using (3) it can be written as

$$v_{ao} = \frac{v_{al} - v_{au}}{2} - \frac{R_a}{2} i_a - \frac{L_a}{2} \frac{di_a}{dt} \tag{4}$$

The upper and lower arm dynamics neglecting the common mode voltage can also be written as

$$-\frac{V_{DC}}{2} + v_{au} + v_{inda} + v_{ao} = 0 \tag{5}$$

$$\frac{V_{DC}}{2} - v_{al} - v_{inda} + v_{ao} = 0 \tag{6}$$

where, v_{inda} is the voltage across arm inductor. Adding (5) and (6),

$$v_{ao} = \frac{v_{al} - v_{au}}{2} \tag{7}$$

The output voltage dynamics of MMC with grid interface is given as

$$v_{ao} = v_{gan} + R_g i_a + L_g \frac{di_a}{dt} \tag{8}$$

where, v_{gan} is grid 'a' phase voltage, L_a is arm inductance, R_a is its internal resistance, L_g is per phase grid inductance and R_g is its internal resistance. Putting (7) in R.H.S and (8) in L.H.S of (4) and rearranging it is written as

$$v_{ao} = v_{gan} + (R_g + \frac{R_a}{2}) i_a + (L_g + \frac{L_a}{2}) \frac{di_a}{dt} \tag{9}$$

$$v_{ao} = v_{gan} + R_{eff} i_a + L_{eff} \frac{di_a}{dt} \tag{10}$$

where, R_{eff} = R_g + $\frac{R_a}{2}$ and L_{eff} = L_g + $\frac{L_a}{2}$. Discretizing (10) and expanding using Eulers approximation, the reference pole voltage v^*_{ao} for output current control is written as

$$v^*_{ao}(k) = v_{gan}(k) + R_{eff} i_a(k) + L_{eff} \frac{i^*_a(k+1) - i_a(k)}{T_s} \tag{11}$$

where, T_s is the sampling time for MPC, $i^*_a(k+1)$ is determined by Lagrange's 2nd order extrapolation. The amplitude of the reference current is provided directly. To deliver power to the grid at unity power factor, the phase angle θ of grid voltage is extracted from synchronous reference based phase locked loop (SRF-PLL) for alignment of the grid phase voltage and the phase ac output current of MMC.

B. 2N+1 Direct Phase Leg PWM

The aim of the modulation stage in this work is to attain reduced switching while ensuring the proper operation of MMC. The per phase reference pole voltage v^*_{ao} is determined in (11) at each carrier underflow. Then it is scaled by $V_{DC}/2N$ and is represented as v^*_{aopu} in Fig. 1(b) for a 7 level MMC along with 6 level shifted sawtooth carriers. The 6 carrier regions and associated indices for a 7 level MMC are indicated in Fig. 1(b) as I_m where m varies from 1 to 6. The reference pole voltage is then mapped as shown in Fig. 1(c) within an innermost single carrier for easier digital implementation. This

is similar to [22] where mapped reference pole voltage is given by

$$v^*_{aopumap} = v^*_{aopu} + (I_m - \frac{n-1}{2}) \tag{12}$$

where, $n = 2N+1$ which is an odd number. This equation is generalized and is applicable for any n-level value.

1) Method 1: Proposed Two-vector PWM scheme: Considering the space vector structure, the two vectors are chosen out of the three vectors forming the vertices of a triangle associated with a particular sector. Some steps need to be followed for finding out the dwell times of the two vectors when the sampled reference value gets carrier compared. In this regard, initially the mapped reference pole voltages of the three phases of MMC are made bipolar as in (13).

$$v^*_{popuadj} = v^*_{popumap} - 0.5 \tag{13}$$

where, p = {a,b,c} and are represented by $v^*_{aopuadj}$, $v^*_{bopuadj}$ and $v^*_{copuadj}$ respectively. The mapped sector information and pivot vectors are found in (14) and (15) respectively at every sampling interval. The mapped sector is termed as sector henceforth for simplicity.

$$\begin{aligned}
v^*_{aopuadj} \geq v^*_{bopuadj} \geq v^*_{copuadj} &= sector-1\\
v^*_{bopuadj} \geq v^*_{aopuadj} \geq v^*_{copuadj} &= sector-2\\
v^*_{bopuadj} \geq v^*_{copuadj} \geq v^*_{aopuadj} &= sector-3\\
v^*_{copuadj} \geq v^*_{bopuadj} \geq v^*_{aopuadj} &= sector-4\\
v^*_{copuadj} \geq v^*_{aopuadj} \geq v^*_{bopuadj} &= sector-5\\
v^*_{aopuadj} \geq v^*_{copuadj} \geq v^*_{bopuadj} &= sector-6
\end{aligned} \tag{14}$$

The pivot vectors V_7 and V_8 are figured out automatically based on three phase sample values and are at the same place as shown in Fig. 2. They are expressed using the combination of the indices as in (15).

$$\begin{aligned}
V_7 &= [(n-I_a),(n-I_b),(n-I_c)]\\
V_8 &= [(n-I_a-1),(n-I_b-1),(n-I_c-1)]
\end{aligned} \tag{15}$$

When the sector information and the pivot vectors' indices are known, the other two vectors V_2 and V_1 (as shown in Fig. 2) forming the other vertices of a triangle can also be easily determined [22]. The three phase reference voltages $v^*_{popuadj}$(representing the vector o′p′ in Fig. 2) is now projected for a particular sector on any one of the particular axis out of a, b and c axes using the expression denoted by va, vb and vc as given in (16). It holds good for other sectors as well.

$$\begin{aligned}
va &= v^*_{aopuadj} - v^*_{bopuadj}cos60^\circ - v^*_{copuadj}cos60^\circ\\
vb &= -v^*_{aopuadj}cos60^\circ + v^*_{bopuadj} - v^*_{copuadj}cos60^\circ\\
vc &= -v^*_{aopuadj}cos60^\circ - v^*_{bopuadj}cos60^\circ + v^*_{copuadj}
\end{aligned} \tag{16}$$

Now, absolute values are taken for all the ac output current errors of the three phases as given below.

$$|i_{perror}| = |i_{pactual} - i_{preference}| \tag{17}$$

where, p = {a,b,c}. The phase with the highest absolute ac output current error out of the three phases is chosen for taking control in a carrier period. The vector switching takes place

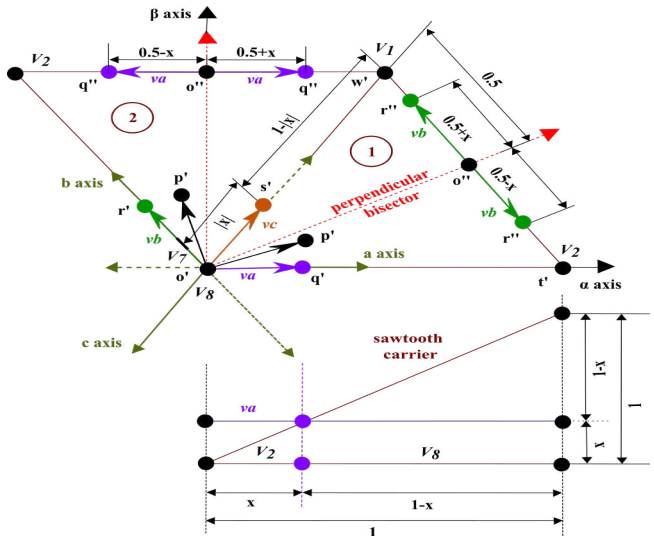

Fig. 2. Projection of per unit adjusted reference voltage in a,b,c axis for $sector-1$ and $sector-2$ with carrier comparison example for 'a' axis.

based on the chosen axis only. Considering $sector-1$, if 'a' axis is chosen, then the two vectors V_8 and V_2 will be applied in a carrier period to achieve va in the average sense. For this, va or $1-va$ as the sampled projected reference is compared with a single level sawtooth carrier. The 'a' axis projected reference voltage value is positive for $sector-1$. However, the start and the end vectors are decided based on the polarity of the output current error to reduce the actual current ripple. If the polarity is positive, then the projected reference is taken as $1-va$ with the start vector as V_8 and if the polarity is negative, then the projected reference is taken as va with the start vector as V_2. If 'b' axis is chosen, vb is either positive or negative with respect to perpendicular bisector and hence to find out the application times of V_1 and V_2, 0.5 need to be adjusted suitably. If 'c' axis is chosen, vc is negative for $sector-1$ as well as for $sector-2$, when $sector-2$ is considered and hence absolute values are taken for carrier comparison. For $sector-2$, va is either positive or negative with respect to perpendicular bisector and vb is positive. The following Table I summarizes the vector application logic for all the sectors where a value is determined for comparing it with a sawtooth carrier.

2) Method 2: Three-vector PWM scheme: The three-vector PWM scheme as in [9] conventionally use three vectors (forming the vertices of a triangle) that are applied in a carrier period to realize the reference voltage vector. The $2N$+1 PD-PWM technique as applied in [13] also expolits the three-vector PWM scheme which is implemented based on simple carrier based comparison method. The triangular carrier is used for the carrier based comparison. As three-vector PWM scheme is widely popular, this is considered as the basis for comparison with the proposed two-vector MMPC scheme for operation of MMC.

TABLE I
DETERMINATION OF SECTOR-WISE VECTOR SWITCHING LOGIC

			If $i_{perror} \geq 0$			$i_{perror} < 0$		
Sector	axis	condition	value	start vector	end vector	value	start vector	end vector
1	a-axis	-	1-x	V_8	V_2	x	V_2	V_8
	b-axis	If $vb \geq 0$	0.5-x	V_2	V_1	0.5+x	V_1	V_2
		If $vb < 0$	0.5+x	V_2	V_1	0.5-x	V_1	V_2
	c-axis	-	1-|x|	V_1	V_7	|x|	V_7	V_1
2	a-axis	If $va \geq 0$	0.5-x	V_2	V_1	0.5+x	V_1	V_2
		If $va < 0$	0.5+x	V_2	V_1	0.5-x	V_1	V_2
	b-axis	-	1-x	V_8	V_2	x	V_2	V_8
	c-axis	-	1-|x|	V_1	V_7	|x|	V_7	V_1
3	a-axis	-	1-|x|	V_1	V_7	|x|	V_7	V_1
	b-axis	-	1-x	V_8	V_2	x	V_2	V_8
	c-axis	If $vc \geq 0$	0.5-x	V_2	V_1	0.5+x	V_1	V_2
		If $vc < 0$	0.5+x	V_2	V_1	0.5-x	V_1	V_2
4	a-axis	-	1-|x|	V_1	V_7	|x|	V_7	V_1
	b-axis	If $vb \geq 0$	0.5-x	V_2	V_1	0.5+x	V_1	V_2
		If $vb < 0$	0.5+x	V_2	V_1	0.5-x	V_1	V_2
	c-axis	-	1-x	V_8	V_2	x	V_2	V_8
5	a-axis	If $va \geq 0$	0.5-x	V_2	V_1	0.5+x	V_1	V_2
		If $va < 0$	0.5+x	V_2	V_1	0.5-x	V_1	V_2
	b-axis	-	1-|x|	V_1	V_7	|x|	V_7	V_1
	c-axis	-	1-x	V_8	V_2	x	V_2	V_8
6	a-axis	-	1-x	V_8	V_2	x	V_2	V_8
	b-axis	-	1-|x|	V_1	V_7	|x|	V_7	V_1
	c-axis	If $vc \geq 0$	0.5-x	V_2	V_1	0.5+x	V_1	V_2
		If $vc < 0$	0.5+x	V_2	V_1	0.5-x	V_1	V_2

C. Circulating current control

The $2N$+1 level two-vector pulse width modulated pole voltage for a 7 level MMC is shown in Fig. 1(d). Here, the upper arm insertion index is N_u and N_l represents the lower arm insertion index of MMC. The arm currents of the three phases are being sensed at every carrier underflow as well as carrier crossing event as the arm currents have faster dynamics which may change substantially between carrier underflow and carrier crossing event. The actual circulating current in phase 'a' is determined from arm current and output current as in (18). It is applicable for other two phases also.

$$i_{cira} = i_{ua} - \frac{i_a}{2} \tag{18}$$

The reference circulating current is compared with i_{cira} at carrier underflow and at carrier crossing events. For the circulating current control, the odd level redundancies are appropriately applied to make the circulating current follow the reference trajectory. A similar circulating current controller as in [10], [13] is used in this work. The instantaneous output phase current information along with the modulating signal is used to inject appropriate dc as well as second harmonic current in order to maintain a tight control on the capacitor voltage deviation around its nominal value of V_{DC}/N.

D. Submodule capacitor voltage balancing

When the upper and lower arm insertion indices in each phase leg of MMC have been determined, the required number of submodules out of N are selected based on their ascending order sorted status and respective arm current polarity. The half bridge submodule capacitor voltages are being sampled once in every carrier period and sorted in ascending order by a conventional sorting algorithm.

TABLE II
SIMULATION AND HARDWARE PROTOTYPE PARAMETERS

Parameter	Simulation	Hardware
Number of submodules in each arm (N)	10	3
DC link voltage (V_{DC})	17 kV	165 V
Rated power (P)	3.06 MW	330 W
Arm Inductance (L_a)	5 mH	3.75 mH
Internal resistance of arm inductor (r_a)	0.1 Ω	0.3 Ω
Output inductance per phase (L_g)	12 mH (grid)	20 mH (standalone)
Output resistance per phase (R_g)	0.2 Ω (grid)	24.4 Ω (standalone)
Submodule capacitance (C_{auj})	2200 μF	1100 μF
Carrier frequency (f_s)	4 kHz	4 kHz
MPC sampling time (T_S)	250 μsec	250 μsec

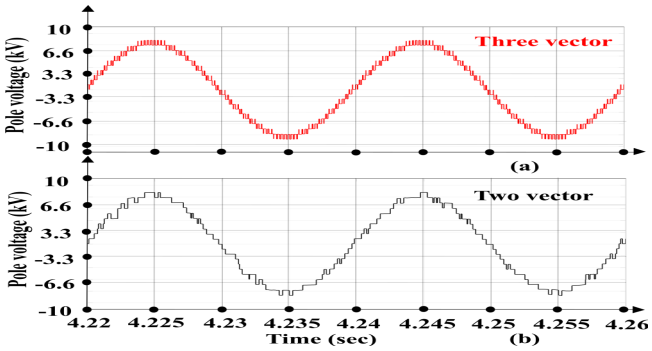

Fig. 3. (a) Three-vector and (b) Two-vector pole voltage for N = 10.

III. SIMULATION RESULTS

The sampling-based simulation is performed on Matlab/Simulink environment for a 21 level (N=10) medium voltage grid connected MMC operating at unity power factor. The simulation parameters are given in Table II. The submodule capacitance and arm inductance values are determined following the guidelines given in [23]. The MMC pole voltage outputs of three-vector and two-vector MMPC schemes are shown in Fig. 3(a) and 3(b) respectively, where direct $2N$+1 phase leg modulation is performed and 21 levels (N=10) of pole voltage of phase 'a' is observed. There is a considerable reduction in the number of state changes or switching events occurring of the pole voltage within a fundamental period for two-vector PWM compared to three-vector PWM. In terms of switching events of pole voltage happening over a fundamental

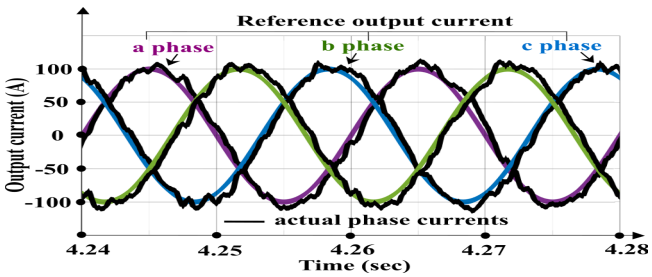

Fig. 4. Three phase output currents of MMC.

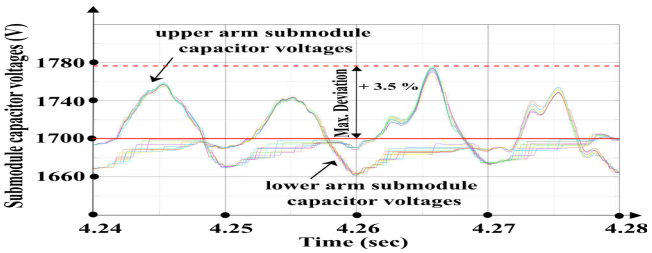

Fig. 5. Capacitor voltages of submodules of phase 'a'.

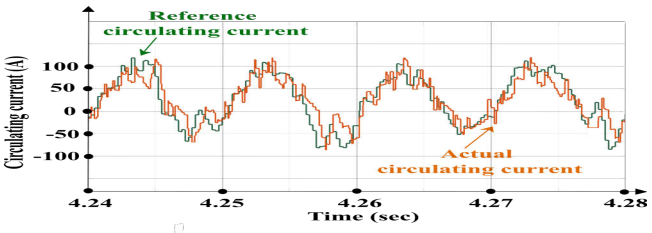

Fig. 6. Inner circulating current control of phase 'a'.

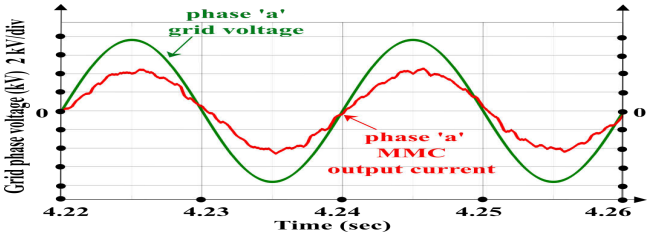

Fig. 7. MMC unity power factor operation.

period, this number is 248 for two-vector PWM in comparison to 594 for three-vector PWM. Hence, the percentage reduction in switching events of pole voltage for two-vector PWM scheme is 58.25 %. The three phase output currents of MMC are shown in Fig. 4. The output current THDs for a two-vector scheme are 4.53 %, 4.63 % and 4.59 % for 'a','b' and 'c' phases respectively, when a 100 A peak sinusoidal current is made to flow into the grid. The output current THDs are within the prescribed IEEE Std. 519 limit (<5%) given in [24]. The upper arm and lower arm submodule capacitor voltages are balanced around V_{DC}/N i.e. 1700 V as depicted in Fig. 5. The maximum submodule capacitor voltage deviation is 3.5 % above the nominal voltage of 1700 V. The circulating current also follows its reference trajectory and the performance of the circulating current controller is shown in Fig. 6. The power, that is delivered to the medium voltage grid by MMC at unity power factor, is evident from phase 'a' grid voltage and output current of MMC being aligned and in phase as in Fig. 7.

IV. Experimental Results

The experimental results are obtained for a 7 level three phase MMC lab prototype when operated in standalone mode with RL load. The control logic was implemented in a combination of TI TMS320F28379D DSP and SPARTAN 6 XC6SLX9 FPGA based boards. The parameters are given in

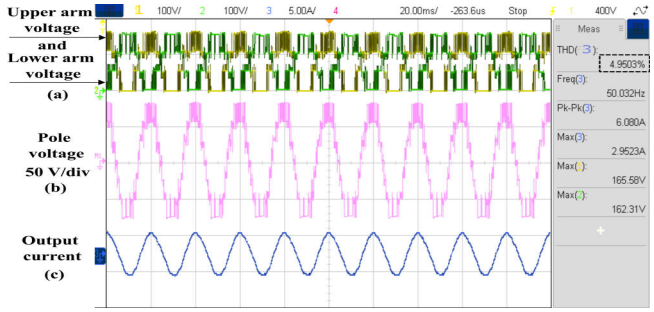

Fig. 8. (a) Upper and lower arm voltage, (b) Pole voltage and (c) Output current for 'a' phase and N=3.

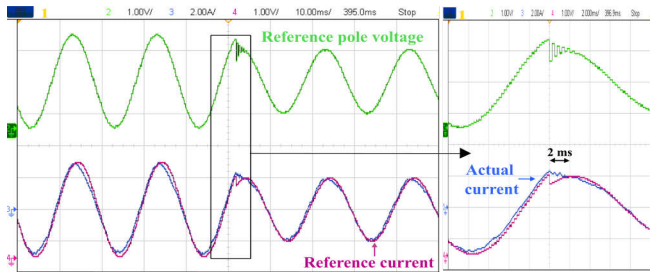

Fig. 9. Dynamic performance of the controller.

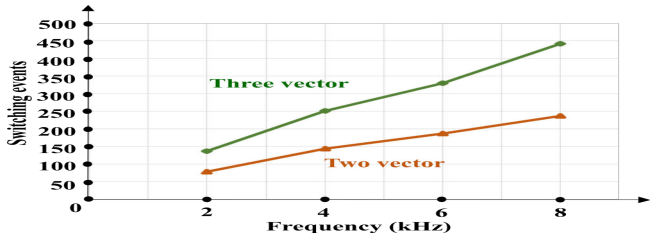

Fig. 10. Three phase MMC switching events comparison over a fundamental period of Three-vector and Two-vector scheme.

Fig. 11. Experimental set-up of 3-ϕ MMC.

Table II. The upper arm and lower arm voltage with 4 levels are shown in Fig. 8(a). The two-vector PWM pole voltage with 7 levels for the 'a' phase is shown in Fig. 8(b). The output current for the corresponding 'a' phase is shown in Fig. 8(c) and the THD value is reported as 4.95 % (for a RL load) on the measurement box of the figure along with other parameters of interest. The transient performance of the current controller

is also presented in Fig. 9 where the reference output current amplitude of 3 A is suddenly changed to 2 A and the actual output current tracks the reference current within 2 $msec$. Fig. 10 shows the combined number of switching events of pole voltages over a fundamental period including all the three phases for both two-vector scheme and three-vector scheme at different switching frequency operations. The percentage reduction is roughly about 42 % to 46 % for a 7 level three phase MMC in hardware.

V. Conclusion

The two-vector MMPC scheme is thoroughly designed and then compared with the conventional three-vector scheme in this work. There is a substantial reduction in switching events in the modulated pole voltage within a fundamental period for the two-vector scheme and the reduction is 58.25 % (for N=10) in simulation and 43 % (for N=3) in hardware for a 4 kHz switching frequency operation when compared to that of three-vector scheme. This will ultimately result in switching loss reduction and thereby improving the efficiency for medium voltage MMC operation. The implementation of MMPC based current control provides a good dynamic performance. A satisfactory performance is observed in controlling the circulating current and maintaining a tight control on the submodule capacitor voltages. The overall two-vector scheme is generalized for any n-level pole voltage operation of MMC and is suitable for digital implementation.

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